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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Sailesh M. Merchant

Serial No.: 09/092,158

Filed: June 5, 1998

For: METHOD FOR THE FABRICATION OF CONTACTS IN AN INTEGRATED CIRCUIT DEVICE

Group: 2823

Examiner: Eaton, K.

Commissioner of Patents
and Trademarks
Washington, D. C. 20231

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APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

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This is an appeal from a Final Rejection dated June 20, 2000, of Claims 1, 2, 4-12, and 14-24. The Appellants submit this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $300.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner

to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 12-2325.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

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I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Lucent Technologies Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1, 2, 4-12, and 14-24 are pending in this Application.

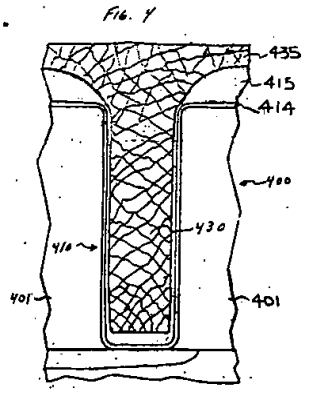
IV. STATUS OF THE AMENDMENTS

The present Application was filed on June 5, 1998. The Appellants filed a first Amendment on March 28, 2000 in response to an Examiner's Action mailed December 28, 1999. The Examiner entered the first Amendment and subsequently issued a Final Rejection on June 6, 2000. The Appellants then filed a Request for Reconsideration on August 15, 2000. The Examiner indicated that the arguments of the Request for Reconsideration were fully considered but did not place the Application in condition for allowance. The Appellants then filed a Notice of Appeal on September 20, 2000.

V. SUMMARY OF THE INVENTION

The present invention is directed, in general, to a method for the fabrication of contact plugs and, more specifically, to a method for the fabrication of tungsten plugs in an integrated circuit device. The present invention provides a method of forming a tungsten plug that exhibits improved contact resistance characteristics in the window provided by a rapid thermal anneal without inducing failure of the Titanium nitride layer. In general and as presently amended, the present invention is directed to method for fabricating a contact in a semiconductor substrate. In the claimed embodiment, the method includes depositing by physical vapor deposition a barrier layer in the contact opening and depositing a contact metal on the barrier layer. A substantial portion of these layers is removed from the surface of the substrate to form the contact plug. The contact plug is then subjected to a rapid thermal temperature anneal sufficient to anneal the barrier layer.

It is important to note that the rapid thermal anneal is performed *after* the removal process, thereby avoiding the damaging effects of performing the rapid thermal anneal immediately subsequent to the deposition of the Ti and TiN films. As depicted in (informal) Figure 4 (set forth herein as Illustration 1), it is important to note that the TiN layer 415 is very thin, approximately 5%-20% of the original field film thickness.



Thus, in one embodiment, the present invention provides a method wherein the rapid thermal anneal is performed after the removal of unwanted portions of W, TiN, and Ti layers, thereby minimizing the exposure of the TiN layer 415 to an angular cross section. Also, since only a fraction of the field thickness is present during the rapid thermal anneal, the advantages of producing $TiSi_x$ at the contact surface 522 during the rapid thermal anneal are achieved while avoiding the damaging effects associated with conventional processes that perform the rapid thermal anneal earlier in the tungsten plug formation process.

VI. ISSUES

A. First Issue Presented for Consideration in this Appeal:

Whether Claims 1, 2, and 4-11, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over the Applicants' admitted prior art in view of U.S. Patent No. 5,827,777 to Schinella, et. al. (Schinella) and U.S. Patent No. 5,462,895 to Chen.

B. Second Issue Presented for Consideration in this Appeal:

Whether Claims 12, and 14-23, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over the Applicants' admitted prior art in view of U.S. Patent No. 5,827,777 to Schinella, et. al. (Schinella) and U.S. Patent No. 5,462,895 to Chen.

C. Third Issue Presented for Consideration in this Appeal:

Whether Claim24, as rejected by the Examiner, is patentably nonobvious in accordance with 35 U.S.C. §103(a) over the Applicants' admitted prior art in view of U.S. Patent No. 5,827,777 to Schinella, et. al. (Schinella) and U.S. Patent No. 5,462,895 to Chen.

VII. GROUPING OF THE CLAIMS

Claims 1, 2, 4-11; 12, 14-23; and 24 do not stand or fall together. Claims 1, 2, and 4-11 are patentably distinct from Claims, Claims 12, 14-23 and Claim 24. Claims 12-23 are patentably distinct from Claims 1,2-11 and Claim 24. Claim 24 forms a third group that is patentably distinct from Claims 1, 2, 4-11 and Claims 12, and 14-23.

VIII. SUMMARY OF REFERENCES RELIED ON

A. Schinella

Schinella is directed to a process for producing a relatively thin titanium nitride (TiN) barrier layer in a contact opening of an integrated circuit. Schinella recognizes the problems associated with the use of tungsten hexafluoride and its effect on the TiN layer within a contact structure during chemical vapor deposition of tungsten. (Col. 3, lines 12-29). Schinella addresses this problem, however, by proposing a method of depositing by physical vapor deposition a very thin layer (e.g., thickness ranging from 50 Å to 200 Å) of TiN. Shinella accomplishes this thin TiN layer by growing the TiN from the previously deposited Ti layer by reactive sputtering in the presence of a nitrogen bearing species. As noted by the Examiner, however, Schinella does not teach or suggest

a step that anneals the Ti/TiN layer after the contact plug formation. The Examiner attempts to cure the deficient teachings of Schinella by combining it with Chen.

B. Chen

Chen, in contrast to the teachings of Schinella, is directed to a chemical vapor deposition method of forming an adhesive layer for a blanket layer that includes a Ti film, a Ti-rich TiN film or a titanium silicide ($TiSi_x$) film or a TiN (stoichiometric) film within a contact opening. The Ti film, Ti-rich TiN film or the $TiSi_x$ film is annealed to be converted into a $TiSi_2$ film (Abstract). It is important to note that Chen uses chemical vapor deposition in all embodiments to achieve the desired amount of deposition. The flow rates that are needed to obtain the proper stoichiometric TiN film are carefully and specifically taught. Furthermore, there is no teaching or suggestion of using another type of deposition technique to achieve the proposed deposition scheme. (Col. 2, lines 15-32 and lines 55-66 and Col. 3, lines 39-54). In fact, Chen teaches that physical vapor deposition (PVD) deposited barrier layers lead to "an increase in the resistance of the contact resistance and diffusion of tungsten into the Si substrate during the annealing." (Column 1, lines 37-46).

IX. THE APPELLANTS' ARGUMENTS

The inventions set forth in independent Claims 1, 12, and 24 and their respective dependent claims are not obvious in view of the references on which the Examiner relies because the references of Schinella and Chen are not properly combined.

A. Rejection of Claims 1, 2, and 4-11 under 35 U.S.C. §103

The Examiner asserts that Schinella discloses a process for the use of titanium nitride layers with tungsten plugs wherein the tungsten is physically vapor deposited immediately after the barrier layer. (Page 4 of the Examiners Action dated December 28, 1999). The Examiner states that Schinella fails to teach or suggest subjecting the contact plug to a temperature sufficient to anneal the barrier layer. (Page 4 of the Examiners Action dated December 28, 1999). To cure this deficiency, the Examiner asserts that Chen discloses a method of making a semiconductor wherein the contact plug is subjected to heat treatment to transform the barrier layer into a lower resistance material. (Page 5 of the Examiners Action dated December 28, 1999). The Examiner believes that it would have been obvious to one skilled in the art to modify the admitted prior art by depositing the tungsten immediately after the barrier layer as taught by Schinella, and further modify this combination by incorporating the heat treatment as taught in Chen. (Page 6 of the Examiners Action dated December 28, 1999). The Applicants respectfully disagree.

It is well established that to establish a prim facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. See MPEP §2143 - §2143.03 for decisions pertinent to each of these criteria.

Because of the disparate teachings of Schinella and Chen, one skilled in the art would not be motivated to combine their teachings. As is well settled, "[o]bviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching

or suggestion supporting the combination." *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572,1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The case law also makes clear that one "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *Ecolochem, Inc. v. So. California Edison*, 56 USPQ2d 1065, 1073 (Fed. Cir. 2000), *In re Fine*, 837 F.2d 1071,1075, 5 USPQ2d 1780, 1783 (Fed. Cir. 1988). Hindsight knowledge of the Applicants' disclose when the prior art does not teach or suggest such knowledge, results in the use of the invention as a template for its own reconstruction. This is inappropriate in the determination of patentability. *Sensonics Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (1983). Moreover, where the inventor has achieved the claimed invention by doing what those skilled in the art suggested should not be done is a fact strongly probative of nonobviousness. *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 19860, on rehearing, 231 USPQ 160 (Fed. Cir. 1986).

The Applicants respectfully submit that one skilled in the art would not be motivated to incorporate the method of annealing taught by Chen with the admitted prior art and Schinella in the manner suggested by the Examiner. First, there is no suggestion or motivation in the references themselves to support their combination. Moreover, the Chen reference teaches away from such a combination.

The admitted prior art and the Schinella reference are directed to methods of forming contact plugs wherein the Ti/TiN layers are deposited by physical vapor deposition (PVD). On the other hand, Chen is concerned with processes that *require* chemical vapor deposition (CVD). One skilled in the art understands that PVD and CVD are not universally interchangeable techniques. Moreover, Chen teaches that PVD-deposited barrier layers lead to "an increase in the resistance of the contact resistance and diffusion of tungsten into the Si substrate during the annealing." (Column

1, lines 37-46). These are undesirable effects. Thus, Chen expressly teaches away from PVD and annealing of the Ti or TiN layers after the tungsten layer has been deposited, as recited in independent Claim 1, which is a strong indication of a lack of motivation to combine, and thus, a strong indication of a lack of obviousness. Furthermore, this annealing is the very teaching of Chen which the Examiner proposes to combine with the PVD techniques of the admitted art and Schinella. Because Chen expressly teaches away from the annealing PVD-deposited layer after the W contact deposition, as proposed by the Examiner, and because the admitted prior art or Schinella employ PVD methods, one skilled in the art would not be motivated to modify the admitted prior art or Schinella by incorporating the annealing step of Chen. Also, it is well settled that a combination of references is improper if the combination would destroy or hinder the functionality of one of the combined devices. If Chen were combined with Schinella, then PVD would be used to deposit the layers, which would, according to Chen, provide an undesirable result. For these reasons, the combination of Chen with the admitted prior art and Schinella is improper.

As admitted by the Examiner, without Chen, the combination of remaining references fail to teach or suggest every element of independent Claim 1. Neither the admitted prior art nor the Schinella reference teaches or suggests, as the Examiner correctly points out, depositing the contact metal immediately after deposition of the barrier layer and prior to the anneal step claimed in the present invention. Similarly, the only reference that teaches annealing the device after depositing the contact metal (Chen), also teaches away from using a *physical vapor deposition* process for forming the barrier layer. Therefore, given that Chen is not properly combined with the admitted prior art, the combination of the admitted prior art and Schinella fails to teach or suggest every element independent Claims 1, 12 and 24.

Additionally, the Appellants respectfully submit that the Examiner's combination of references disassembles the Appellants' invention into its constituent elements, attempts to find each element in the prior art and then asserts that it is easy to incorporate these individual elements. This constitutes improper hindsight. The Examiner is not allowed to use the Appellants' disclosure as a blue print to reconstruct the claimed invention out of isolated teachings in the prior art. *Grain Processing Corp. v. American Maize-Products Co.*, F.2d 902, 907, 5 USPQ2d 1788, 1792 (Fed. Cir. 1988). This is clearly the situation since not only do the references lack a motivation to combine, but also disclose an express teaching away from their combination. Thus, because the references are improperly combined, and because the Examiner has stated that the remaining references fail to teach or suggest each element of the Appellants' claimed invention, the Examiner has failed to establish a prima facie case of obviousness with respect to independent Claim 1. Because Claims 2 and 4-11 depend upon independent Claim 1, the Examiner has also failed to establish a prima facie case of obviousness with respect to these dependent claims, which the Applicants pointed out to the Examiner during prosecution. Moreover, the Examiner has also failed to offer any additional evidence to the contrary to overcome the Applicant's successful rebuttal of the Examiner's prima facie case of obviousness.

As previously stated Claims1, 2, 4-11 do not stand or fall together with Claims 12, 14-23 and Claim 24. The Appellants' position is based on the fact that Claims 1, 2, and 4-11 include different elements than those found in Claims 12, 14-23 and Claim 24.

B. Rejection of Claims 12, and 14-23 under 35 U.S.C. §103

The Examiner has rejected these claims based on the combined teachings of the admitted prior art, Schinella, and Chen. Claim 12, on which Claims 14-23 depend from, includes similar

elements to those recited in Claim 1, plus additional elements not present in Claim 1. As previously discussed, the admitted prior art, Schinella and Chen are improperly combined. Therefore, any rejection based on this combination fails to establish a prima facie case of obviousness for the same reasons as set forth above. Moreover, without Chen, as the Examiner has stated, the admitted prior art individually or in combination with Schinella fails to teach or suggest the elements recited in Claim 12 or its dependent Claims 14-23. Thus, these references also fail to establish a prima facie case of obviousness. As such, Claims 14-17 and 19-23 are not obvious in view of the admitted prior art, Schinella, or Chen.

As previously stated, Claims 12 and 14-23 do not stand or fall together with Claims 1, 2, and 4-11 and Claim 24. The Appellants' position is based on the fact that Claims 12 and 14-23 include different elements than those found in Claims 1, 2, and 4-11 and Claim 24.

C. Rejection of Claim 24 under 35 U.S.C. §103

The Examiner has rejected these claims based on the combined teachings of the admitted prior art, Schinella, and Chen. Claim 12, on which Claims 14-23 depend from, includes similar elements to those recited in Claim 1, plus additional elements not present in Claim 1. As previously discussed, the admitted prior art, Schinella and Chen are improperly combined. Therefore, any rejection based on this combination fails to establish a prima facie case of obviousness. Moreover, without Chen, as the Examiner has stated, the admitted prior art individually or in combination with Schinella, fails to teach or suggest the elements recited in Claim 12 or its dependent Claims 14-23. Thus, these references also fail to establish a prima facie case of obviousness. As such, Claims 14-17 and 19-23 are not obvious in view of the admitted prior art, Schinella, or Chen.

As previously stated, Claim 24 does not stand or fall together with Claims 1, 2, and 4-11 and Claims 12 and 14-23. The Appellants' position is based on the fact that Claim 24 includes different elements than those found in Claims 1, 2, and 4-11 and Claims 12 and 14-23.

For the reasons set forth above, the Claims on appeal are patentably nonobvious over the combination of Schinella and Chen. Accordingly, the Appellant respectfully requests that the Board

of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellant's pending claims.

Respectfully submitted,

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X. APPENDIX A - CLAIMS

1. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening;

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

2. The process of Claim 1 wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer.

4. The process of Claim 1 wherein said depositing said barrier layer includes depositing said barrier layer in said contact opening formed in a dielectric and having an aspect ratio ranging from about 3:1 to about 5:1.

5. The process of Claim 1 wherein said depositing a contact metal includes depositing tungsten.

6. The process of Claim 5 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

7. The process of Claim 1 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process.

8. The process of Claim 1 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

9. The process of Claim 8 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

10. The process of Claim 8 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

11. The process of Claim 10 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

12. A process for fabricating an integrated circuit, comprising:

forming an active device on a semiconductor substrate;

forming a contact opening in a dielectric deposited on said active device, said contact opening in electrical contact with said active device;

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening;

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

14. The process of Claim 13 wherein said depositing includes depositing said titanium layer and said titanium nitride layer by physical vapor deposition.

15. The process of Claim 12 wherein said forming said contact opening includes forming said contact opening having an aspect ratio ranging from about 3:1 to about 5:1.

16. The process of Claim 12 wherein said depositing a contact metal includes depositing tungsten.

17. The process of Claim 16 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

18. The process of Claim 12 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process for a period ranging from about 5 seconds to about 60 seconds, a temperature of said rapid thermal anneal process ranging from about 600°C to about 750°C.

19. The process of Claim 12 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

20. The process of Claim 19 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

21. The process of Claim 19 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

22. The process of Claim 21 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

23. The process of Claim 12 wherein forming said active device includes forming an active device having a design width of about 0.25 microns or less.

24. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.